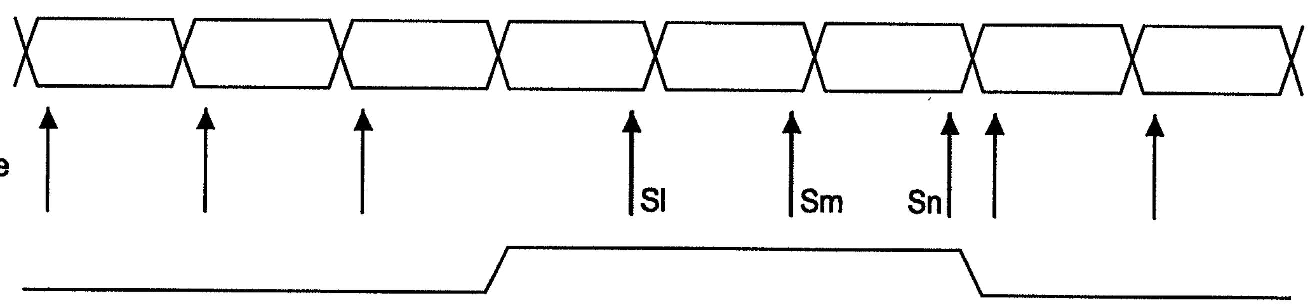


Fig.1A DUT Output

Fig.1B Tester Strobe

Fig.1C Shift

Fig.2A DUT Clock Input

Fig.2B DUT Output

Fig.2C Tester Strobe Point

Fig.2D DUT Delay :L→ H

Fig.2E DUT Delay : H→L

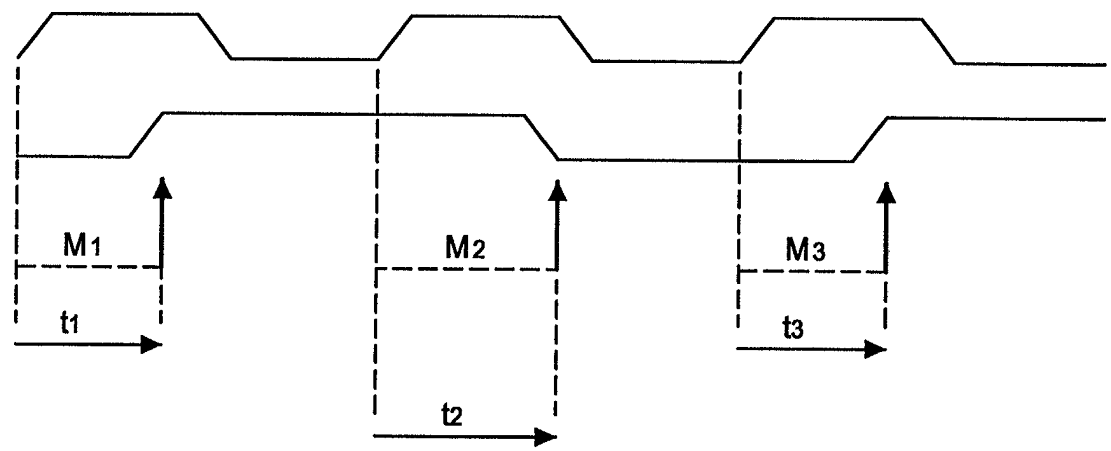
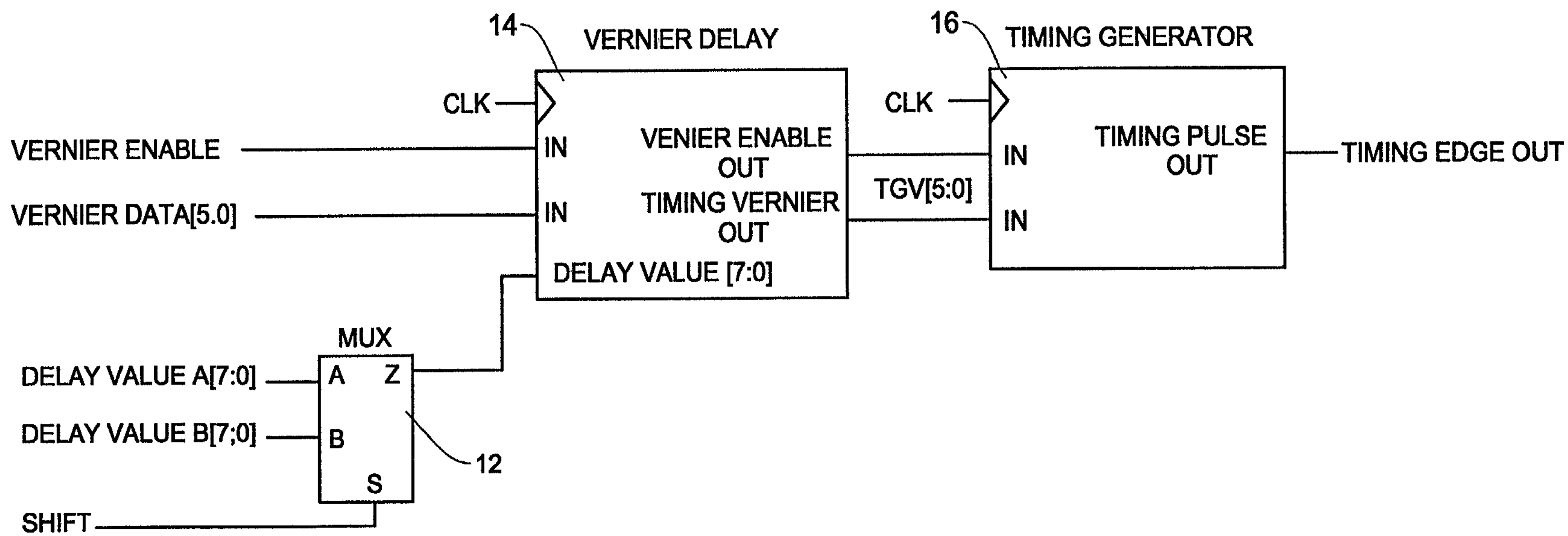


Fig.3



14
VERNIER DELAY
16
TIMING GENERATOR
CLK
IN
VENIER ENABLE OUT
IN
TIMING VERNIER OUT
DELAY VALUE [7:0]
CLK
IN
TGV[5:0]
IN
TIMING PULSE OUT
TIMING EDGE OUT
VERNIER ENABLE
VERNIER DATA[5.0]
MUX
A
Z
B
S
12
DELAY VALUE A[7:0]
DELAY VALUE B[7;0]
SHIFT

Fig.4A

Fig.4B

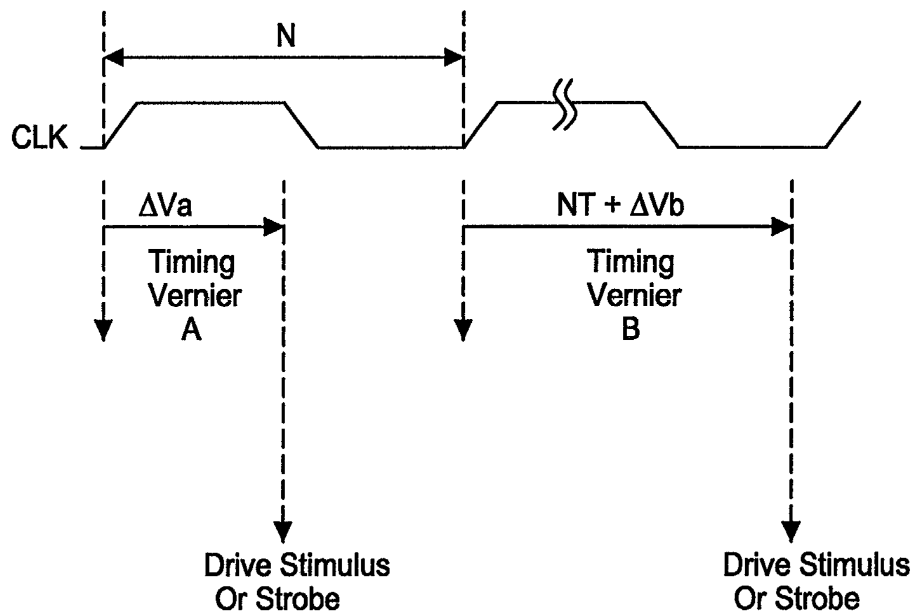
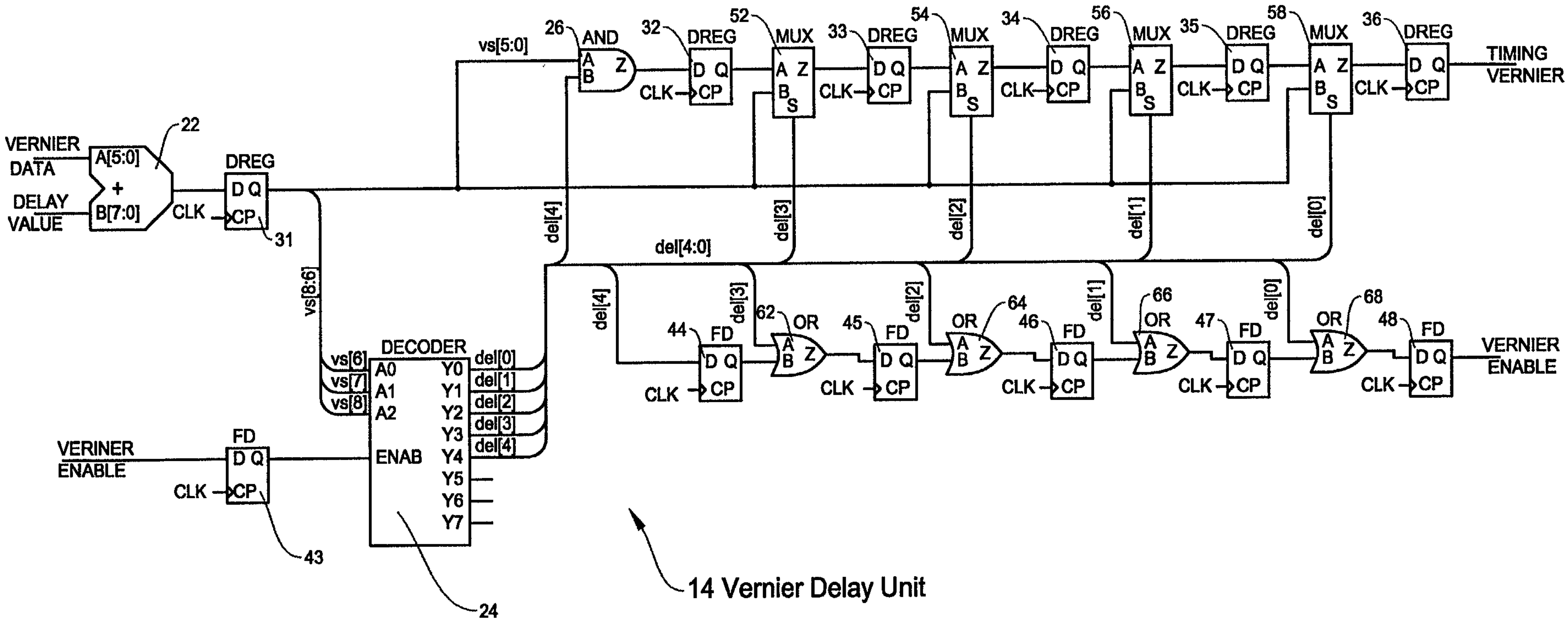

N
CLK
ΔVa
Timing
Vernier
A
NT + ΔVb
Timing
Vernier
B
Drive Stimulus
Or Strobe
Drive Stimulus
Or Strobe

Fig.5



VERNIER DATA
DELAY VALUE
A[5:0]
B[7:0]
+
22
DREG
D Q
CLK
CP
31
vs[5:0]
vs[8:6]
26
AND
A
B
Z
32
DREG
52
MUX
33
54
34
56
35
58
36
S
TIMING VERNIER
del[4]
del[3]
del[2]
del[1]
del[0]
del[4:0]
DECODER
vs[6]
vs[7]
vs[8]
A0
A1
A2
ENAB
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
VERINER ENABLE
FD
43
24
44
62
OR
45
64
46
66
47
68
48
VERNIER ENABLE
14 Vernier Delay Unit

Fig.6

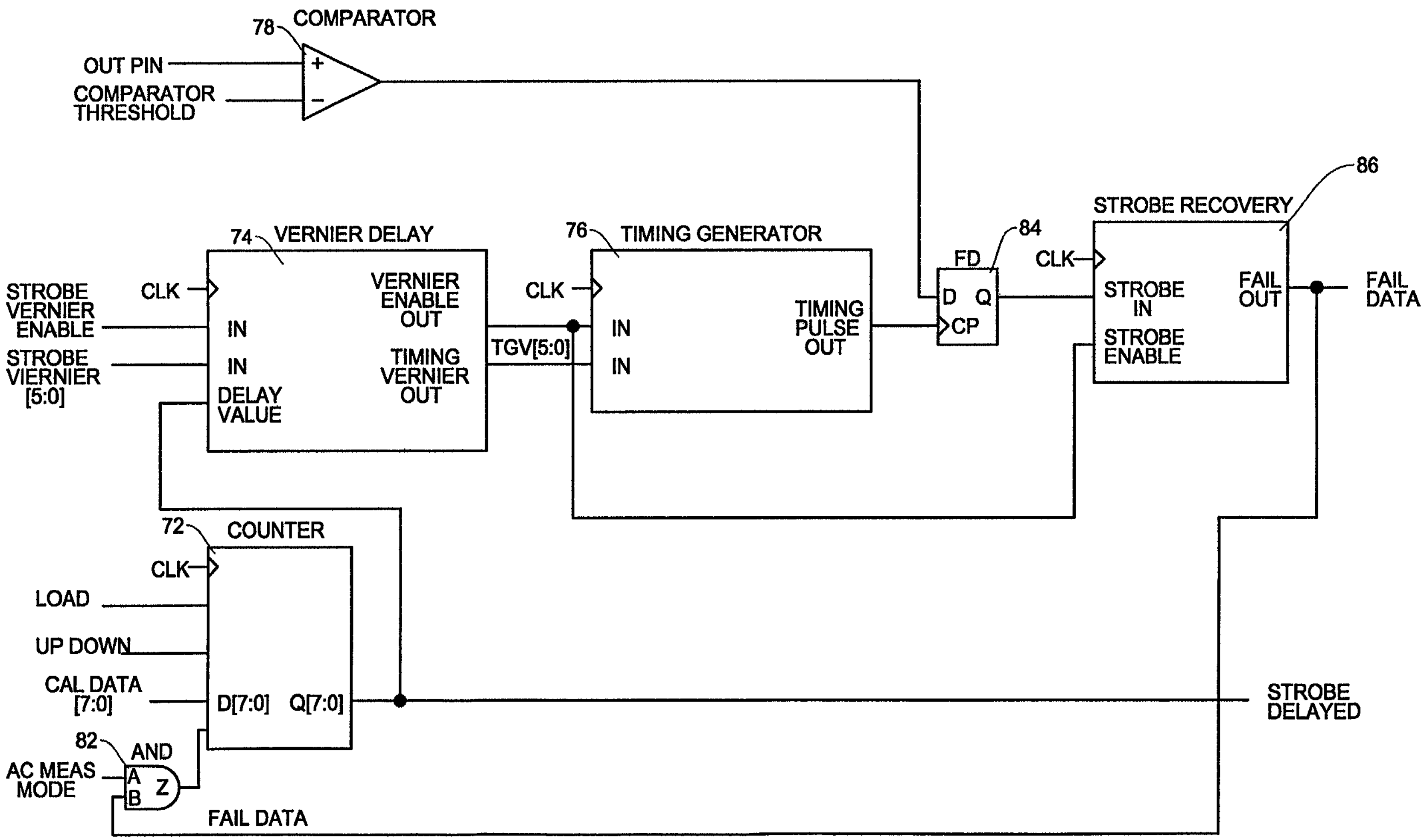
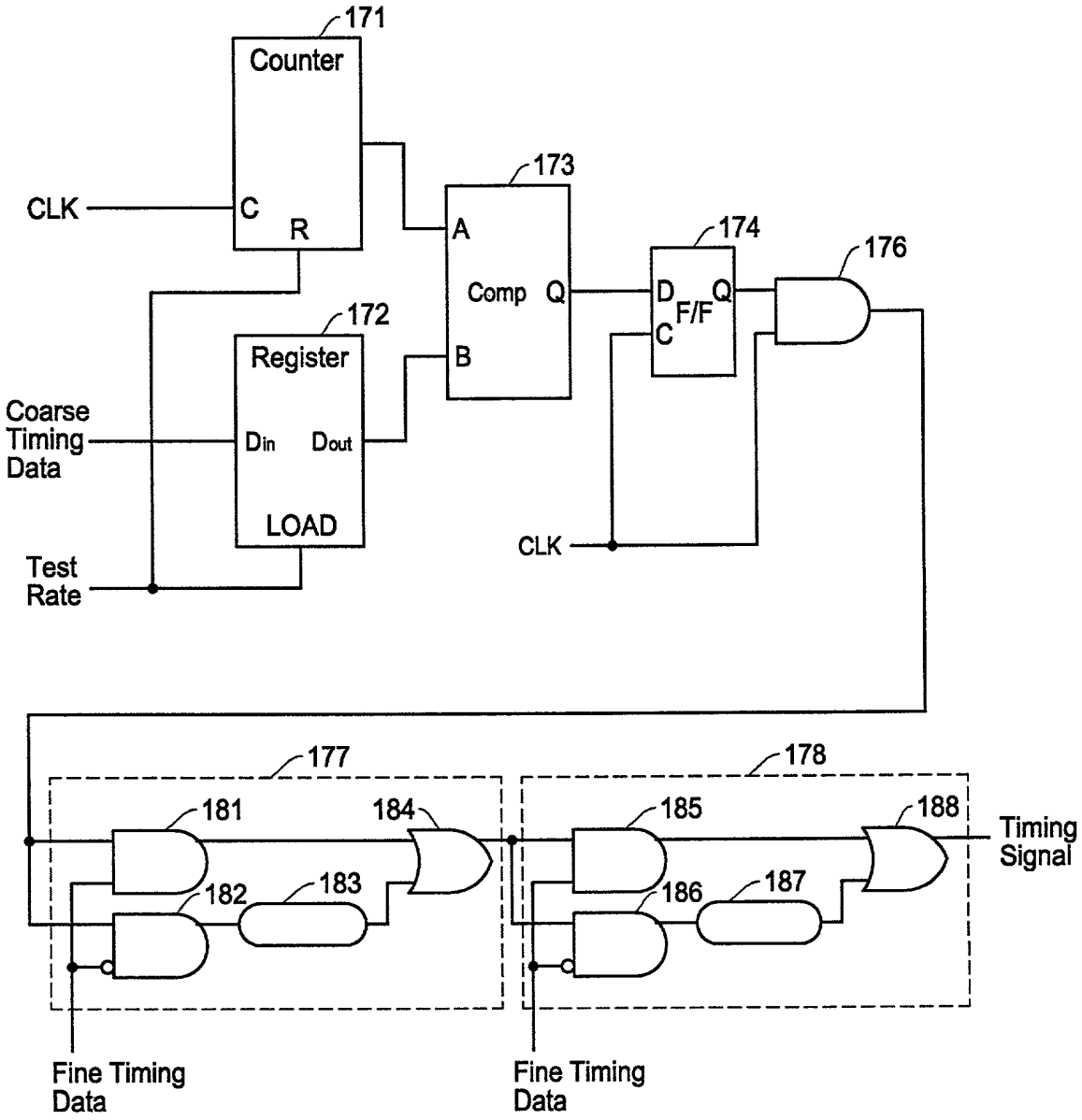

78
COMPARATOR
OUT PIN
COMPARATOR THRESHOLD
+
−
74
VERNIER DELAY
CLK
STROBE VERNIER ENABLE
STROBE VIERNIER [5:0]
IN
IN
DELAY VALUE
VERNIER ENABLE OUT
TIMING VERNIER OUT
TGV[5:0]
76
TIMING GENERATOR
CLK
IN
IN
TIMING PULSE OUT
84
FD
D
Q
CP
86
STROBE RECOVERY
CLK
STROBE IN
STROBE ENABLE
FAIL OUT
FAIL DATA
72
COUNTER
CLK
LOAD
UP DOWN
CAL DATA [7:0]
D[7:0]
Q[7:0]
STROBE DELAYED
82
AND
AC MEAS MODE
A
B
Z
FAIL DATA

FIG. 7


171
Counter
CLK
C
R
173
A
Comp
Q
B
174
D
F/F
Q
C
176
172
Register
Coarse
Timing
Data
Din
Dout
LOAD
Test
Rate
CLK
177
178
181
184
185
188
Timing
Signal
182
183
186
187
Fine Timing
Data
Fine Timing
Data